50 includes an illustrative gate insulation layer **50**A and an illustrative gate electrode **50**B. As will be recognized by those skilled in the art after a complete reading of the present application, the gate structure **50** of the device **100** depicted in the drawings, i.e., the gate insulation layer **50**A and the gate electrode **50**B, is intended to be representative in nature. For example, the gate insulation layer **50**A may be comprised of a variety of different materials, such as, for example, silicon dioxide, a so-called high-k (k greater than 10) insulation material (where k is the relative dielectric constant), etc. The gate electrode **50**B may be comprised of one or more layers of conductive material, e.g., polysilicon, one or more layers of metal, etc. As noted above, in some cases, if desired, a metal layer (not shown), such as a very thin work function adjusting metal (e.g., a layer of titanium nitride), may be formed on the high-k gate insulation layer **50**A. As will be recognized by those skilled in the art after a complete reading of the present application, the insulating materials and the metal layer(s) that are part of the replacement gate structure **50** may be of any desired construction and comprised of any of a variety of different materials. Additionally, the replacement gate structure **50** for an NFET device may have different material combinations as compared to a replacement gate structure **50** for a PFET device. Thus, the particular details of construction of replacement gate structure **50**, and the manner in which such replacement gate electrode structure **50** is formed, should not be considered a limitation of the present invention unless such limitations are expressly recited in the attached claims.

[0039] In one illustrative example, the replacement gate formation process begins with performing a conformal deposition process to form the high-k gate insulation layer **50**A in the gate cavity **40** and above the layer of insulating material **30**. Thereafter, the conductive materials that will be used for the gate electrode **50**B, e.g., one or more metal layers, will be deposited across the devices by performing one or more conformal deposition processes and/or one or more blanket-deposition processes so as to substantially overfill the gate cavity **40** with conductive gate electrode material(s). At that point, one or more CMP processes are performed to remove excess portions of the gate insulation layer **50**A and the layers of conductive material that will be used to form the gate electrode **50**B are positioned above the layer of insulating material **30**. This CMP process essentially planarizes the upper surface of the materials of the gate structure **50** with the upper surface of the layer of insulating material **30**. Thereafter, an etching process is performed to reduce the height of the replacement gate structure **50** such that the upper surface **50**S of the replacement gate electrode **50**B is positioned below the upper surface **20**S of the first sacrificial sidewall spacers **20**.

[0040] Next, as shown in FIG. **2**M, an illustrative gate cap layer **52**, comprised of, for example, silicon nitride, has been formed above the recessed gate structure **50**. The gate cap layer **52** may be formed by depositing a layer of the cap material and thereafter performing a CMP process to remove excess portions of the cap material positioned on top of the layer of insulating material **30**.

[0041] Then, as shown in FIG. **2**N, an etching process **54** is performed to remove the residual portions of the first and third sacrificial sidewall spacers **20**, **38**. The etching process **54** results in the formation of second spacer cavities or low-k spacer cavities **54**A adjacent the replacement gate structure **50**. More specifically, the etching process **54** exposes the sidewall **50**W of the replacement gate structure **50**, i.e., it exposes the gate insulation layer **50**A. The etching process **54** may be a dry or wet etching process. In the illustrative case where the first and third sacrificial sidewall spacers **20**, **38** are made of carbon, the etching process may be performed using a mild plasma chemistry, such as, for example, oxygen-based ashing with mild power, or a wet H_2O_2/H_2SO_4 based chemistry.

[0042] FIG. **2**O depicts the device **100** after a plurality of low-k sidewall spacers **60** have been formed in the second spacer cavities **54**A adjacent the replacement gate structure **50**. The structure depicted in FIG. **2**O is the result of several process operations. Initially, in one embodiment, a layer of low-k insulating material (not shown) is blanket-deposited across the device **100** above the layer of insulating material **30**. Thereafter, excess portions of the low-k insulating material positioned outside of the second spacer cavities **54**A may be removed by performing a dry etch-back process or by performing a CMP process. As used herein and in the claims, as it relates to the formation of the low-k spacers **60**, the term "low-k material" or "low-k spacer" should be understood to mean any material having a dielectric constant less than that of traditional spacer material—silicon nitride, i.e., "low-k spacer" or "low-k material" means a material with a k value less than 7. Some illustrative materials that may be used for the low-k spacers **60** include, for example, SiCN, SiBN, SiOCN and SiBCN. The low-k material for the low-k spacers **60** may be formed by performing a CVD process, an ALD process, etc. Note that, in this example, the low-k spacers **60** are formed after the source/drain anneal processes have been performed on the device **100** so the low-k spacers **60** will not be degraded by being subjected to such an anneal process. Additionally, in the depicted embodiment, the low-k spacers **60** actually engage the gate insulation layer **50**A of the replacement gate structure **50**. More specifically, the gate insulation layer **50**A depicted herein has a generally "U" shaped configuration with a substantially horizontal portion **51**H (that contacts the substrate **10**) and two upstanding vertically oriented (relative to the surface of the substrate) portions **51**V. In the depicted example, the inside surface **61** of the low-k spacers **60** engages the vertically oriented portions **51**V of the gate insulation layer **50**A along substantially the entire length (in the vertical direction normal to the surface of the substrate **10**) of the vertical portions **51**V of the gate insulation layer **50**A.

[0043] At the point of fabrication depicted in FIG. **2**O, traditional manufacturing operations may be performed to complete the formation of the device **100**. For example, contact openings (not shown) may be formed through the layers of insulating material **30**, **28**R, **26** to expose the underlying source/drain regions **24**. Thereafter metal silicide regions (not shown) may be formed on the exposed portions of the source/drain regions **24** and conductive contacts (not shown) may be formed in the contact openings to provide electrical connection to the source/drain regions **24**. Various metallization layers may then be formed above the device **100** using known processing techniques.

[0044] FIGS. **2**P-**2**Q depict another illustrative embodiment disclosed herein. FIG. **2**P corresponds to the point of fabrication depicted in FIG. **2**I wherein the wet etching process **34** is performed to remove the residual portions of the second sacrificial sidewall spacers **22** and the layer of insulating material **26**, i.e., the etching process **34** removes exposed silicon nitride material while leaving the first sacrificial sidewall spacers **20** intact. The etching process **34**